New thermally enhanced packages for power MOSFETs in battery pack applications

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Abstract

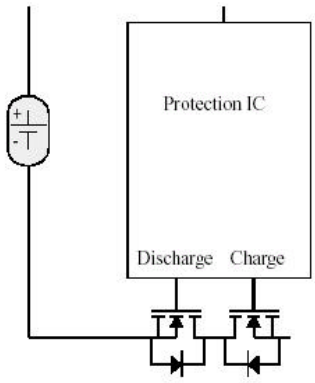
Recent advances in silicon technology have enabled smaller, higher-efficiency devices by increasing the transistor cell density on the silicon level to 178 million cells per square inch. These silicon capabilities represent a major advance over the devices available just a few years ago, and it is important that advances in packaging technology keep pace.

Because of the demanding power and size requirements of next-generation portable devices, new compact packages with superior current-handling capabilities will be increasingly important. In this article, a new thermally enhanced package technology from Vishay Siliconix will be introduced for use in cellular phone 1-2 cell Li+ battery-protection circuits. With the die attach copper pad soldered directly to the printed circuit board, this new packaging technique provides a direct, low-resistance thermal path to the substrate on which the device is mounted.

Characteristics of thermally enhanced 1212-8 package will be compared to that of the industry standard TSSOP-8 package through review of the MOSFET packaging trends used in today's battery pack protection circuits.

Introduction

Recent years have seen the remarkable spread of mobile phones, PDAs, and other mobile devices whose functions and performance are advancing with increasing speed. To address all of these challenges, the world market for high-density rechargeable batteries also has entered a transitional phase. Lithium Ion (Li+) and Lithium Polymer (LiP) batteries are rapidly replacing Nickel Cadmium (NiCd) and Nickel Metal Hydride (NiMH) batteries. For today's cellular phone, a single-cell Li+ cell is often the battery of choice due to its small size and high energy density. Li+ cells are generally suited to a constant-current/constant-voltage charging strategy, and although relatively simple to implement, charging the cell actually requires precise control of the "float voltage" region in order to obtain the maximum capacity with long cell life. In summary, if the voltage is too low, the cell will not be fully charged; if the voltage is too high, the cycle life is significantly degraded. In addition, excessive over- and under-charge of a



Li+ cell can result in catastrophic failure of the unit.

The key to preventing these effects from occurring is to add protection circuitry into the battery pack, which typically contains a control IC, two back-to-back battery-protection MOSFETs, and a gas gauge IC to monitor the charge status of the battery pack (Figure 1).

Figure 1. A typical Li+ protection circuit

To cope with the demand for slim-looking mobile devices, the technological trend for battery cells is also to create thinner and lighter batteries. As the batteries get smaller, the components in the protection circuit boards that are attached to one plane of the battery cells should follow the same design rules. In an effort to meet this increasing need for power density, many discrete power semiconductor manufacturers have been introducing several new packaging techniques. In this paper, we will analyze the impact of one of these new packaging approach used for power MOSFET devices by comparing it to some of the older generation packages commonly used in the battery pack applications today. Although there are many ways to do that comparison (such as On-resistance ($r_{DS(on)}$ per unit area, component dimensions (size, height), $P_{D,}$ etc.); in this paper, we will evaluate the *thermal characteristics* of various packages for this purpose.

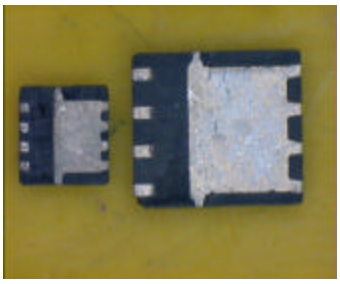


Figure 2. PowerPAK 1212-8 and PowerPAK SO-8

Thermal Performance of MOSFET Packages

A MOSFET generates internal heat due to the current passing through the channel. This self-heating raises the junction temperature of the device above that of the PCB to which it is mounted, causing significant increase in power dissipation of the device. A major source of this problem lies in the large values of junction-to-foot thermal resistance of the MOSFET package. A common request for power MOSFETs in today's battery pack protection circuits is to have the lowest $r_{DS(on)}$ in smallest package. The purpose of this paper is to show that, in any design, engineers must also take into account the change in MOSFET $r_{DS(on)}$ with temperature and hence thermal capability of the package as well.

A basic measure of a device's thermal performance is the junction-to-case thermal resistance, Rθjc, or the junction-to-foot thermal resistance, Rθjf. This parameter is measured for the device mounted to an infinite heat sink and is therefore a characterization of the device only. In other words, it is independent of the properties of the board to which the device is mounted.

A new package technology addresses the increasing demand for ultra-low thermal impedance in a small package that is ideal for space-constrained applications. (Figure 2). The bottom of the die attach pad is exposed to provide a direct, low-resistance thermal path to the substrate on which the device is mounted. In other words, the main thermal path is no longer through the leads but through a large area of copper pad. (Figure 3).

As a result, thermal resistance is significantly improved. Figure 4 shows a table comparing the Rθjc of various packages to steady-state value. The improvement in thermal resistance for the new package types is obvious. θ_{J-A} is defined as the device soldered to a 1-inch square FR4 board with copper on both sides. Note that the thermal performance of thermally enhanced 1212-8 and standard SO-8 packages

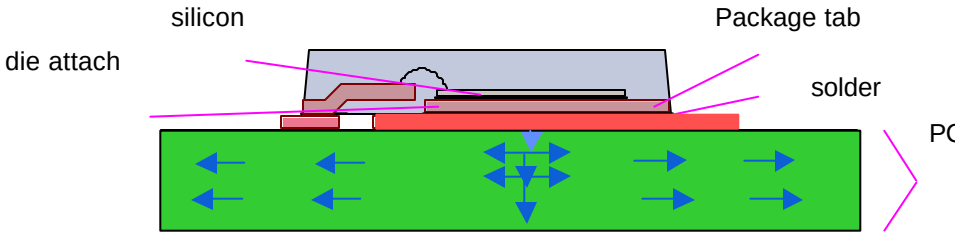
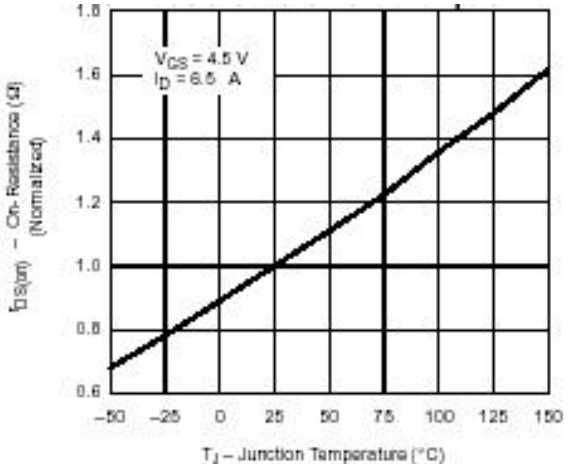


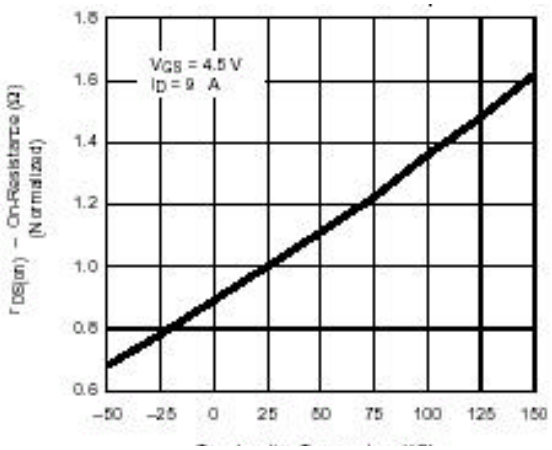
Figure 3. The PowerPAK allows utilization of the PCB's natural heatsink ability.

are almost equivalent. The equivalence is due the leadless package construction, which provides a heat conduction path directly from the die downward to the foot. A similar approach, eliminating the leads to provide a direct thermal pad, can be observed in many new packages now being introduced by discrete component manufacturers.

Package	RT_{J-C}	RT_{J-A}
DPAK	1.8°C/W	50°C/W
PowerPAK SO-8	**1.2°C/W**	**50°C/W**
Standard SO-8	20°C/W	80°C/W
PowerPAK SO-8	**2.4°C/W**	**81°C/W**
TSSOP-8	45°C/W	115°C/W

Figure 4. Package Thermal Performance of various MOSFET packages





Quite often designers will have to add more copper to the drain pad of a power MOSFET to improve the heat conduction from the device. For optimum performance, it is helpful to understand the improvement afforded by a given area of “spreading copper.” For that purpose, thermally enhanced 1212-8 devices were mounted on a 2-in.sq. four-layer FR4 PCB. The two internal layers and the backside layer are solid copper. The top layer was progressively cut back to a smaller area, and at each step, junction-to-ambient thermal resistance measurements were taken. These results indicated that no additional thermal performance improvement was realized above an optimum area of 0.2 in.sq. to 0.3 in.sq. A subsequent experiment was conducted in which the copper on the backside was removed, first in stripes to mimic the circuit traces and then entirely. No significant effect was observed under either condition.

To explain the impact of that characteristic on the current handling capability of power MOSFET devices we evaluated two Common Drain N-channel power MOSFETs using the same size silicon manufactured by same silicon technology. (As junction-to-case thermal resistance, $R_{\theta jc}$ is a function of die area, we, therefore, eliminated the impact of die size from the calculations). The measurements clearly indicated that the current handling capability of the thermally enhanced 1212-8 MOSFET (measured as 9A) was about 39% better than the MOSFET packaged in TSSOP-8 using the same silicon (measured as 6.5A) under similar conditions. (Figure 5).

To apply the thermal characteristics of various packages into real applications, let’s consider four different MOSFET devices in different packages mounted on a PC board with a board temperature of 45°C (Figure 6). Also let’s suppose that each device is dissipating 2 W. Using the junction-to-foot thermal resistance characteristics of the the thermally enhanced 1212-8 and the other SMT packages, die temperatures are determined to be 49.8°C for the thermally enhanced 1212-8, 85°C for the standard SO-8, 149°C for the standard TSSOP-8, and 1125°C for the TSOP-6. This is a 4.8°C rise over the board temperature for the thermally enhanced 1212-8, and a rise of more than 40°C for other SMT packages. *A 4.8°C rise has a minimal effect on on-resistance, whereas a rise of more than 40°C will cause an increase in on-resistance as high as 20%.*

By minimizing the junction-to-foot thermal resistance, the MOSFET die temperature is very close to the temperature of the PCB. Bringing

the junction temperature down will increase the die efficiency by around 20% compared with TSSOP-8. As power dissipation is a function of T_j (junction temperature) and Rθjc (junction-to-case thermal resistance) following the simple formula:

$$P_D = \frac{T_{j,max} - 25}{R_{th,JC}}$$

the lower the Rθjc value, the higher would be the power dissipation of the package increasing the efficiency of the design.

The continuous improvements in silicon technology helped to achieve lower on-resistance for power MOSFET devices. This has enabled designers to reduce the package sizes significantly for a given application requirement. The very same practice has been applied to the MOSFETs used in battery-pack protection circuits. New MOSFET devices can provide the performance of a TSSOP-8 in a 40% smaller footprint (9 mm^2 for the thermally enhanced 1212-8 versus 19.2 mm^2 for the TSSOP-8). The extra circuit volume freed up by using smaller packages instead of the TSSOP-8 can be used to store extra energy, improving the efficiency of the design significantly. From a consumer's standpoint, this will mean significant improvements in talk time and standby time for cellular phone applications. It was clear from the thermal measurements we did on various power MOSFET packages that the efficiency of designs can be improved significantly by putting more emphasis on the thermal characteristics of the package chosen for the application. Obviously this becomes quite important and handy considering the increasing demand for efficiency required by the next generation cellular phones and other portable devices.

CONCLUSIONS

Steady state thermal resistance, Rθjc, is the thermal resistance between a semiconductor device's junction and a specified reference part on the device's case or package. Rθjc values represent a baseline upon which drain current, I_D, and device power dissipation, P_D values are derived. The lower the Rθjc values, the higher will be the I_D and P_D values respectively, which means a much more efficient design.

By minimizing the thermal rise above the board temperature, this packaging technique simplifies thermal design considerations that keep the on-resistance low and permits the device to handle more current than a same- or larger-size power MOSFET die in a standard TSSOP-8 or SO-8 package.

It is recommended that the design engineers working on battery pack protection circuits to pay more attention to the thermal characteristics of the power MOSFETs they select for their applications to increase the efficiency and robustness of their design.

REFERENCES:

1. Zhao, Johnson, PowerPAK-1212 Mounting and Thermal Considerations, Vishay Siliconix AN822, August 2001
2. Vishay Siliconix power MOSFET datasheets (www.vishay.com)

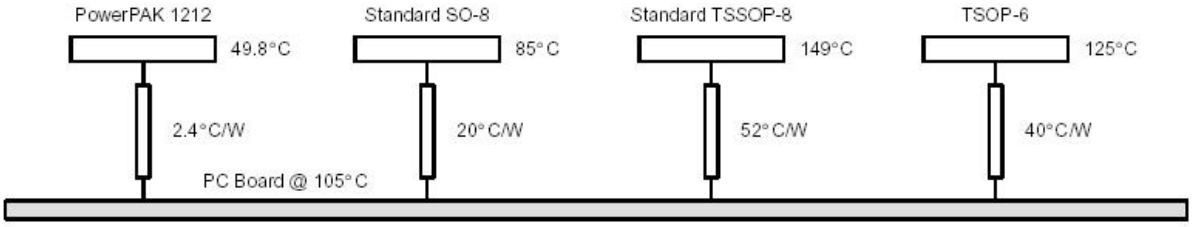


Figure 6. Temperature of various packages on a PCB